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(54) Method of manufacturing the circuit device and circuit device

(57) After a trench 54 is formed in a first conductive foil 60A, the circuit elements are mounted, and the insulating resin is applied on the laminated conductive foil 60 as the support substrate. After being inverted, a second conductive foil 60B is etched on the insulating resin 50 as the support substrate for separation into the conductive paths. Accordingly, it is possible to fabricate the circuit device in which the conductive paths 51 and the circuit elements 52 are supported by the insulating resin 50, without the use of the support substrate. And the interconnects L1 to L3 for the circuit are formed, and can be prevented from slipping because of the curved structure and a visor 58.

FIG.1A

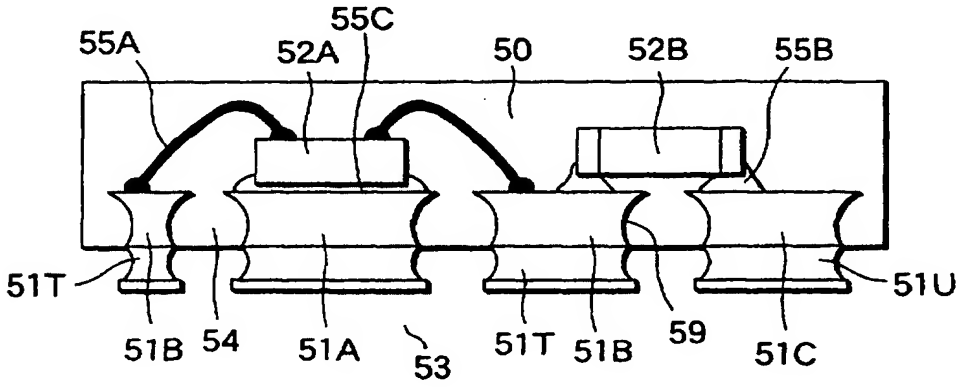

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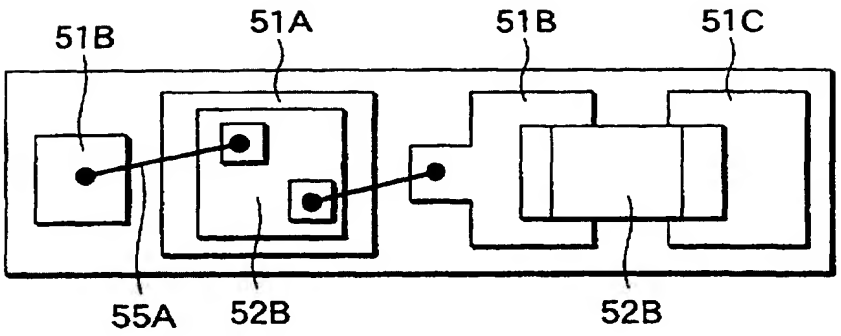
FIG.1B



Description

[0001] The present invention relates to a method of manufacturing a circuit device and the circuit device, and more particularly to a method for manufacturing a thin-type circuit device.

[0002] Conventionally, it has been demanded that a circuit device which is set in an electronic apparatus is reduced in size, thickness and weight, because the circuit device is used for a portable telephone, a portable computer and so on.

[0003] For example, a semiconductor device as a circuit device is typically a package type semiconductor device which is conventionally sealed by normal transfer molding. This semiconductor device 1 is mounted on a printed circuit board PS as shown in Fig. 24 of the accompanying drawings.

[0004] This package type semiconductor device 1 has a semiconductor chip 2 covered with a resin layer 3, with a lead terminal 4 for external connection derived from the side of this resin layer 3.

[0005] However, this package type semiconductor device 1 had the lead terminal 4 out of the resin layer 3, and was too large in total size to meet smaller, thinner and lighter requirements.

[0006] Therefore, various companies have competed to develop a wide variety of structures which are reduced in size and weight. Recently, a wafer scale CSP which is as large as a chip size, called a CSP (Chip Size Package), or a CSP which is slightly larger than the chip size, has been developed.

[0007] Fig. 25 shows a CSP 6 which adopts a glass epoxy substrate 5 as a support substrate and which is slightly larger than a chip size. Herein, a transistor chip T is mounted on the glass epoxy substrate 5.

[0008] On the surface of this glass epoxy substrate 5, a first electrode 7, a second electrode 8 and a die pad 9 are formed, and on the back face, a first back electrode 10 and a second back electrode 11 are formed. Via a through hole TH, the first electrode 7 and the first back electrode 10, as well as the second electrode 8 and the second back electrode 11, are electrically connected. On the die pad 9, the bare transistor chip T is fixed. An emitter electrode of transistor and the first electrode 7 are connected via a bonding wire 12, and a base electrode of transistor and the second electrode 8 are connected via the bonding wire 12. Further, a resin layer 13 is provided on the glass epoxy substrate 5 to cover the transistor chip T.

[0009] The CSP 6 adopts the glass epoxy substrate 5, which has the merits of a simpler structure extending from the chip T to the back electrodes 10, 11 for external connection, and a less expensive cost of manufacture, than the wafer scale CSP.

[0010] The CSP 6 is mounted on the printed circuit board PS, as shown in Fig. 24. The printed circuit board PS is provided with the electrodes and wires making up an electric circuit, and has the CSP 6, the package type semiconductor device 1, a chip resistor CR and a chip capacitor CC fixed for the electrical connection.

[0011] A circuit on this printed circuit board is packaged in various sets.

[0012] Referring to Figs. 26 and 27, a method for manufacturing this CSP will be described below. In Fig. 27, reference is made to a flow diagram entitled as a Glass epoxy/flexible substrate, listed in the middle.

[0013] Firstly, the glass epoxy substrate 5 is prepared as a base material (support substrate) . On both sides of the glass epoxy substrate 5, the Cu foils 20, 21 are applied via an insulating adhesive (see Fig. 26A).

[0014] Subsequently, the Cu foils 20, 21 corresponding to the first electrode 7, the second electrode 8, the die pad 9, the first back electrode 10 and the second back electrode 11 are coated with an etching resist 22 and patterned. Note that the patterning may be made separately on the front face and the back face (see Fig. 26B).

[0015] Then, using a drill or a laser, a hole for the through hole TH is opened in the glass epoxy substrate. This hole is plated to form the through hole TH. Via this through hole TH, the electrical connection between the first electrode 7 and the first back electrode 10 and between the second electrode 8 and the second back electrode 10 is made (see Fig. 26C).

[0016] Further, though being not shown in the figure, the first electrode 7 and the second electrode 8 which become the bonding posts are subjected to Ni plating, and the die pad 9 which becomes a die bonding post is subjected to Au plating to effect die bonding of the transistor chip T.

[0017] Lastly, the emitter electrode of the transistor chip T and the first electrode 7, and the base electrode of the transistor chip T and the second electrode 8 are connected via the bonding wire 12, and covered with the resin layer 13 (see Fig. 26D).

[0018] As required, individual electrical elements are formed by dicing. In Fig. 26, only one transistor chip T is provided on the glass epoxy substrate 5, but in practice, a matrix of transistor chips T are provided. Accordingly, a dicing apparatus separates them into individual elements.

[0019] In accordance with the above manufacturing method, a CSP type electrical element using the support substrate 5 can be completed. This manufacturing method is also effected with the use of a flexible sheet as the support substrate.

[0020] On the other hand, a manufacturing method adopting a ceramic substrate is shown in a flow diagram to the left in Fig. 27. After the ceramic substrate which is the support substrate is prepared, the through holes are formed. Then using a conductive paste, the electrodes are printed and sintered on the front face and the back face. Thereafter, the same manufacturing method of Fig. 26, up to coating the resin layer is followed, but since the ceramic substrate is very fragile, and is likely to break off, unlike a flexible sheet or the glass epoxy

substrate, there is a problem with the difficulty of molding using a metal mold die. Therefore, a sealing resin is potted and cured, then polished for the uniform treatment of the sealing resin. Lastly, using the dicing apparatus, individual devices are made.

[0021] In Fig. 25, the transistor chip T, connecting means 7 to 12, and the resin layer 13 are requisite components for the electrical connection with the outside, and the protection of transistor. However, only these components were difficult to provide an electrical circuit device reduced in size, thickness and weight.

[0022] Essentially, there is no need of having the glass epoxy substrate 5 which becomes the support substrate, as described before. However, since the manufacturing method involves pasting the electrode on the substrate, the support substrate is required, and this glass epoxy substrate 5 could not be dispensed with.

[0023] Accordingly, the use of this glass epoxy substrate 5 raised the cost. Further, since the glass epoxy substrate 5 was thick, the circuit device was thick, limiting the possibility to reduce the size, thickness and weight of the device.

[0024] Further, the glass epoxy substrate or the ceramic substrate necessarily requires a through hole forming process for connecting the electrodes on both sides. Hence, there was a problem with the long manufacturing process.

[0025] Fig. 28 shows a pattern diagram on the glass epoxy substrate, the ceramic substrate or a metal substrate. On this pattern, an IC circuit is typically made, with a transistor chip 21, an IC chip 22, a chip capacitor 23 and/or a chip resistor 24 mounted. Around this transistor chip 21 or the IC chip 22, a bonding pad 26 integral with a wire 25 is formed to electrically connect the chips 21, 22 with the bonding pad via a bonding wire 28. A wire 29 is made integrally with an external lead pad 30. These wires 25, 29 are bent through the substrate, and made slender in the IC circuit, as necessary. Accordingly, this slender wire has smaller contact area with the substrate, leading to exfoliation or curvature of the wire. The bonding pad 26 is classified into a bonding pad for power and a bonding pad for small signal. Particularly, the bonding pad for small signal has a small bonding area, which caused a film exfoliation.

[0026] Further, an external lead is fixed to an external lead pad 30. There was a problem that the external lead pad might be exfoliated due to an external force applied to the external lead.

SUMMARY OF THE INVENTION

[0027] The present invention intends to manufacture a reliable and accurate circuit device easily.

[0028] The present invention has been achieved in the light of the above-mentioned problems, and its object is to provide a method for manufacturing a circuit device, comprising,

forming a conductive path patterned in a predetermined shape by patterning a surface layer of a plate,
electrically connecting a desired circuit element with said desired conductive path,
coating said circuit element and said conductive path with an insulating resin, and
exposing said conductive path by removing said plate from an opposite surface of the conductive path.

[0029] According to the above method, at bonding step, since bonding region of said conductive path has high regidity and can be kept to be at original position, bonding reliability is very high. Further at molding step, since bonding region of said conductive path also has high regidity and can be kept to be at original position, short circuit can be suppressed efficiently.

[0030] According to the above method, positioning accuracy is improved and an accurate and reliable circuit board can be obtained.

[0031] For example, as a starting material, conductive material which mainly includes copper, copper foil is used, sheet resistance is smaller and wiring resistance can bee reduced in comparison with a film formed by plating. Further since copper foil is normally formed by extension process under pressure, even if there is difference of thermal expansion coefficient, it is difficult to cause a crack and bonding characteristic can be improved. In comparison with that, in the case that plating film is used, since plating film is grown in orientation with Z axis, it is weak for extension stress to z direction. Therefore plating film has a disadvantage, that crack is easy to be generated by extension stress for face direction and bonding characteristic is bad.

[0032] The present invention has been achieved in the light of the above-mentioned problems, and its object is to provide a method for manufacturing a circuit device, comprising,

supporting a conductive path patterned in a predetermined shape and having a curved lateral face with a conductive foil,
electrically connecting and fixing a desired circuit element on said desired conductive path,
coating said circuit element and said conductive path with an insulating resin, and
removing said conductive foil excluding at least a portion corresponding to said conductive path.

[0033] With this manufacturing method, the through hole can be dispensed with, the effective use of the conductive foil is made to serve as the support substrate and the conductive path, with the minimum number of components, the conductive path being prevented from slipping off the insulating resin.

[0034] Further according to the method, since sufficient bonding area can be secured and resin invades

between the conductive paths, short circuit can be suppressed.

[0035] For example in the case that material mainly includes copper, such as a copper foil, is used as a starting material, the side edges are covered with thin oxide film, such as Cu_2O,CuO, is formed uniformly. In the case that the side edges are curved, the surface area is especially large, chemical bonding ability with epoxy resin is very good. Therefore adherence of conductive path with resin is highly improved.

[0036] According to a third aspect of the invention, there is provided a method for manufacturing a circuit device, comprising the steps of,

preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil,
forming a first conductive path of curved structure on the lateral face by forming a trench in said first conductive foil excluding at least a region for the conductive path;
electrically connecting and fixing a desired circuit device on said desired first conductive path;
coating and molding said circuit device and said first conductive path with an insulating resin to be filled into said trench; and
removing said second conductive foil at a portion corresponding to said trench and forming a second conductive path on the back face of said first conductive path.

[0037] The second conductive foil is utilized as an etching stopper in forming the first conductive path, and prevents the first conductive path from breaking up. And it is used as the second conductive path ultimately. The insulating resin filled into the trench supports the conductive path integrally to prevent slippage of the conductive path. Of course, the through hole can be also dispensed with.

[0038] According to a fourth aspect of the invention, there is provided a method for manufacturing a circuit device, comprising the steps of,

preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil,
forming a corrosion resistant conductive coat on at least a region which becomes a conductive path on the surface of said first conductive foil,
forming a first conductive path of curved structure on the lateral face by forming a trench in said conductive foil excluding at least a region for the conductive path,
fixing a circuit element on said desired first conductive path,
forming connecting means for electrically connecting an electrode of said circuit element with said desired first conductive path,
coating and molding said circuit element, said connecting means and said first conductive path with an insulating resin to be filled into said trench, and fitting said conductive path and said insulating resin, and
removing said second conductive foil which is not provided with said trench, and forming a second conductive path on the back face of said first conductive path.

[0039] The second conductive foil is utilized as an etching stopper in forming the first conductive path, and prevents the first conductive path from breaking up. And it is used as the second conductive path ultimately. The use of the conductive coat forms a visor on the surface of the conductive path. Due to the insulating resin covering this visor and filled into the trench, the conductive path is prevented from slipping. Of course, the through hole can be also dispensed with.

[0040] According to a fifth aspect of the invention, there is provided a method for manufacturing a circuit device, comprising the steps of,

preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil,
forming a conductive path of curved structure on the lateral face by forming a trench in said first conductive foil excluding at least a region for the conductive path,
fixing a circuit element on said desired conductive path,
forming connecting means for electrically connecting an electrode of said circuit element with said desired first conductive path,
coating and molding said circuit element, said connecting means and said first conductive path with an insulating resin to be filled into said trench, and fitting said first conductive path and said insulating resin,
removing said first conductive foil which is not provided with said trench, and forming a second conductive path on the back face of said first conductive path, and
severing said insulating resin for separation into individual circuit devices.

[0041] According to a sixth aspect of the invention, there is provided a method for manufacturing a circuit device, comprising the steps of,

preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil,
forming a corrosion resistant conductive coat on at least a region which becomes a conductive path on the surface of said first conductive foil,
forming a conductive path of curved structure on the

lateral face by forming a trench in said first conductive foil excluding at least a region for the first conductive path,
fixing a circuit element on said desired first conductive path,
forming connecting means for electrically connecting an electrode of said circuit element with said desired first conductive path,
coating and molding said circuit element with an insulating resin to be filled into said trench, and fitting said first conductive path and said insulating resin,
removing said second conductive foil which is not provided with said trench, and forming a second conductive path on the back face of said first conductive path, and
severing said insulating resin for separation into individual circuit devices.

[0042] The invention will be further described by way of example with reference to the accompanying drawings, in which:-

Fig. 1 is a view for explaining a circuit device according to the present invention.

Fig. 2 is a view for explaining the circuit device of the invention.

Fig. 3 is a view for explaining a method for manufacturing the circuit device of the invention.

Fig. 4 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 5 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 6 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 7 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 8 is a view for explaining the circuit device of the invention.

Fig. 9 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 10 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 11 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 12 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 13 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 14 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 15 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 16 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 17 is a view for explaining the circuit device of the invention.

Fig. 18 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 19 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 20 is a view for explaining the method for manufacturing the circuit device of the invention.

Fig. 21 is a view for explaining a circuit device of the invention.

Fig. 22 is a view for explaining a circuit device of the invention.

Fig. 23 is a view for explaining a way of mounting the circuit device of the invention.

Fig. 24 is a view for explaining a mounting structure of the conventional circuit device.

Fig. 25 is a view for explaining the conventional circuit device.

Fig. 26 is a view for explaining a method for manufacturing the conventional circuit device.

Fig. 27 is a view for explaining the method for manufacturing the conventional circuit device and the circuit device of the present invention.

Fig. 28 is a pattern diagram of an IC circuit which is applicable to the conventional circuit device and the circuit device of the invention.

Fig. 29 is a diagram for explaining the relation between the semiconductor manufacturer and the set maker.

First embodiment for circuit device

[0043] Referring to Fig. 1, a circuit device of the present invention will be first described below in con-

nection with its structure.

[0044] Fig. 1 shows a circuit device 53 in which a conductive path 51 is buried into an insulating resin 50, and a circuit element 52 is fixed on said conductive path 51 supported by the insulating resin 50. The lateral face of the conductive path 51 has a curved structure 59.

[0045] This circuit device 53 is mainly composed of the circuit elements 52A, 52B, the first conductive paths 51A to 51C, and the insulating resin 50 into which the first conductive paths 51A to 51C are buried. Between the first conductive paths 51A to 51C, a trench 54 is filled with the insulating resin 50. And the insulating resin 50 supports the conductive path 51 of the curved structure 59.

[0046] Furthermore, the conductive path 51 is substantially laminated. Namely, a first conductive path 51A and a second conductive path 51S, a first conductive path 51B and a second conductive path 51T, and a first conductive path 51C and a second conductive path 51U are laminated.

[0047] The insulating resin may be a thermosetting resin, such as epoxy resin, or a thermoplastic resin, such as polyimide resin and polyphenylene sulfide. Also, the insulating resin may be any of the resins as far as they can be set by the use of a mold, or coated by dipping or application.

[0048] The laminated conductive foil has a structure, for example, in which the first conductive path on the upper layer is made of Cu (or Al) as the main constituent, and the second conductive path on the lower layer is made of Al (or Cu) as the main constituent. The upper layer and lower layer can be constituted by a same material.

[0049] Connecting means for the circuit elements 52 may be a bonding wire 55A,a conductive ball made of brazing material, an oblate conductive ball, a brazing material 55B such as solder, a conductive paste 55C such as Ag paste, a conductive coat, or an anisotropic conductive resin. These connecting means may be selected depending on the kind of the circuit element 52, and the mounting mode of the circuit element 52. For example, for the bare semiconductor element, a metallic bonding wire is selected to connect the electrode on the surface and the conductive path 51. For the CSP or flip chip, a solder ball or solder bump is selected. For the chip resistor or chip capacitor, the solder 55B is selected. The circuit element packaged, for example, a BGA or package type semiconductor device, can be mounted in the conductive path 51 without causing any problem, in which the connecting means may be solder.

[0050] To fix the circuit element with the conductive path 51A, an insulating adhesive is selected if the electrical connection is unnecessary. If the electrical connection is required, the conductive coat is adopted. Herein, at least one layer of conductive coat may be required.

[0051] The conductive coat materials may be Ni, Ag, Au, Pt or Pd, which is coated by evaporation, sputtering or CVD under low vacuum or high vacuum, plating, or sintering the conductive paste.

[0052] For example, Ag is adherent to Au, as well as the brazing material. Hence, if an Au coat is applied on the back face of the chip, the chip can be directly subjected to thermocompression bonding with an Ag coat, Au coat or solder coat on the conductive path 51A, or the chip can be fixed via the brazing material such as solder. Herein, such conductive coat may be formed on the uppermost layer of the conductive coats laminated. For example, on the conductive path 51A of Cu, two layers of Ni coat and Au coat may be applied in due order, three layers of Ni coat, Cu coat and solder coat applied in due order, or two layers of Ag coat and Ni coat applied in due order. Note that a number of other kinds of conductive coat or lamination structures are considered, but omitted here.

[0053] This circuit device has the insulating resin 50 for covering the conductive path 51 and filled into the trench 54 between the first conductive paths 51A to 51C to support them integrally.

[0054] The interval between these conductive paths 51 is the trench 54 where the insulating resin 50 is filled, and has the merit of effecting insulation between them.

[0055] The interval between the conductive paths 51A to 51C with the curved structure 59 is the trench 54 where the insulating resin 50 is filled, and the merit of preventing the conductive paths 51A to 51C from slipping and effecting insulation between them.

[0056] This circuit device has the insulating resin 50 for covering the circuit elements 52 to be filled into the trench 54 between the conductive paths 51A to 51C, and supporting the conductive paths integrally with the second conductive paths 51S to 51U exposed.

[0057] By exposing the second conductive paths 51S to 51U, the back face of the second conductive paths can be connected with the external. Hence, there is a feature that the conventional through hole of Fig. 25 can be dispensed with.

[0058] In the case where the circuit elements are directly fixed via the conductive coat made of brazing material, Au, or Ag, the heat developed by the circuit elements or the conductive path 52A can be transferred to the mounting substrate via the conductive path 51A. Particularly by heat release, this circuit element is effective for the semiconductor chips which can improve the characteristics such as increased drive current.

[0059] In Fig. 1, a plurality of circuit elements constitute an IC circuit, and the conductive paths for connection between the circuit elements are wired, with a land configuration as shown in Fig. 1B. However, the practical configuration is more complex as shown in Figs. 2 and 28.

Second embodiment for circuit element

[0060] A circuit element 53 of Fig. 2 will be described below.

[0061] This circuit element has substantially the same structure as that of Fig. 1, except that the interconnects L1 to L3 are formed as the conductive path. Accordingly, the interconnects L1 to L3 will be described below.

[0062] As described before, there are a wide variety of IC circuits from a small-scale circuit to a large-scale circuit. For the convenience of the drawings, the small-scale circuit is only shown in Fig. 2A. This circuit is most applicable to an audio amplifying circuit having a difference amplifying circuit and a current mirror circuit connected. The difference amplifying circuit is constituted of TR1 and TR2, and the current mirror circuit is constituted of TR3 and TR4, as shown in Fig. 2A.

[0063] Fig. 2B is a plan view of the circuit element to which the circuit of Fig. 2A is applied. Fig. 2C is a cross-sectional view taken along the line A-A in Fig. 2B. Fig. 2D is a cross-sectional view taken along the line B-B. To the left of Fig. 2B, a die pad 51A for mounting the TR1 and TR3 is provided. To the right of Fig. 2B, a die pad 51D for mounting the TR2 and TR4 is provided. On the upper side of the die pads 51A, 51D, there are provided the electrodes for external connection 51B, 51E to 51G, and on the lower side thereof, there are provided the electrodes for external connection 51C, 51H to 51J. Note that reference signs B, E denote a base electrode and an emitter electrode, respectively. Since a TR1 emitter and a TR2 emitter are commonly connected, an interconnect L2 is formed integrally with the electrodes 51E, 51G. Also, since a TR3 base and a TR4 base, as well as a TR3 emitter and a TR4 emitter are commonly connected, an interconnect L1 is formed integrally with the electrodes 51C, 55J, and an interconnect L3 is formed integrally with the electrodes 55H, 55I.

[0064] There is a feature that the interconnects L1 to L3 correspond to the interconnects 25 and 29 in Fig. 28. These interconnects are different depending on the degree of integration of this circuit element, and have the width as narrow as 25μm or more. Note that this width of 25μm is a numerical value taken when the wet etching is used. If the dry etching is used, its width can be narrower.

[0065] As will be clear from Fig. 2D, a first conductive path 51K constituting the interconnect L1 is buried into the insulating resin 50, and has a lateral face of curved structure which is supported by the insulating resin 50. In other words, the interconnect is buried into the insulating resin 50. Hence, the wires can be prevented from slipping or warping, unlike the wires simply pasted on the support substrate as shown in Figs. 24 to 28. Particularly, since the lateral face of the first conductive path is a rough face with curved structure, and the visor is formed on the surface of the first conductive path, there is an anchor effect to prevent the conductive path from slipping off the insulating resin, as will be apparent from a manufacturing method hereinafter described. The structure of visor will be described later in Fig. 8.

[0066] The electrodes 51B, 51C, 551E to 51J for external connection are buried into the insulating resin, as described previously. Therefore, even if an external force is applied via an external lead secured therein, the electrodes are unlikely to be peeled. Herein, a resistor R1 and a capacitor C1 are omitted, but may be mounted on the first conductive path. As will be described in the later embodiment of the mounting structure, they may be mounted on the back face of this circuit element, or externally mounted on a printed circuit board.

Third embodiment for circuit device

[0067] A circuit device of Fig. 8 will be described below.

[0068] This circuit device has substantially the same structure of Fig. 1 or 2, except that a conductive coat 57 is formed on the surface of the first conductive paths 51A to 51C. Herein, the conductive coat 57 will be mainly described below.

[0069] A first feature is to provide an anchor effect owing to a second material which is different from a material of the first conductive paths 51A to 51C (hereinafter referred to as a first material). Since a visor 58 is formed by the second material, and applied with the first conductive paths 51A to 51C which are buried into the insulating resin 50, the anchor effect is developed to prevent the first conductive path 51 from slipping.

[0070] In the present invention, both the curved structure 59 and the visor 58 develops the double anchor effect to suppress the slippage of the first conductive paths 51A to 51C.

[0071] In the above three embodiments, there has been described the circuit device having a plurality of circuit elements mounted and the wires included to constitute the circuit. However, the present invention is also applicable to a circuit device which is constituted of one circuit element (semiconductor device or passive element) sealed therein, as shown in Figs. 21 and 22. Fig. 21 shows the circuit device in which a face down element 80 such as CSP or flip chip is mounted. Fig. 22 shows the circuit device in which a passive element 82 such as a chip resistor or chip capacitor is sealed. Further, the bonding wire may be provided between two conductive paths and sealed therein. This is usable as a fuse.

First embodiment for a manufacturing method of a circuit device

[0072] Referring to Figs. 3 to 7 and Fig. 1, a manufacturing method of a circuit device 53 will be described below.

[0073] Firstly, as shown in Fig.3a sheet conductive foil 60 is prepared. This conductive foil 60 is composed of a first conductive foil 60A and a second conductive foil 60B which are laminated.

[0074] It is important here that both conductive foils can be selectively etched and the value of resistance is low. To increase the degree of integration, it is also im-

portant that a fine pattern can be formed in etching. For example, when the first conductive foil 60A is patterned by etching, the second conductive foil 60B acts as an etching stopper. Also, when the second conductive foil 60B is patterned as the second conductive path by etching, the first conductive foil 60A is not etched.

[0075] For example, the low resistive materials may include Cu, Al, Au, Ag or Pt. In view of the cost and workability, Cu and Al are preferable. Cu is the most preferable material because it has low resistance and is cheap, and can be subjected to wet etching. Accordingly, to pursue the low cost and low resistance value, it is preferable that Cu is used as the first conductive foil 60A. However, Cu is less liable to dry etching. On the other hand, Al is mostly used for the wires of semiconductor IC, and can be etched by anisotropic etching. Because the lateral face can be etched directly, the higher density of wire can be attained. Accordingly, to pursue the finer pattern, Al may be adopted as the first conductive foil 60A.

[0076] For example, when Cu is adopted as the first conductive foil, an Al foil is prepared. Cu is plated on the surface of this Al foil, so that the thickness of Cu can be adjusted to have the finer pattern. If the thickness of Cu is reduced, the etching in the traversal direction does not proceed, so that the finer pattern can be made. When Al is used as the first conductive foil 60A, a Cu foil is prepared. On this Cu foil, Al is made by deposition or sputtering, enabling the film thickness of Al to be adjusted. Further, since the anisotropic etching can be effected by a C12 gas or a mixture of C12 gas and BCl3 gas, the finer pattern can be made.

[0077] The laminated conductive foil 60 is adopted for explanation below in which the second conductive foil 60B is an Al foil having a thickness of 10μm to 300μm, and the first conductive foil 60A plated with Cu several μm to about 20μm in thickness is laid on the second conductive foil 60B.

[0078] The sheet laminated conductive foil 60 is rolled in a desired width, and may be carried to each process as will be described later, or may be cut in a predetermined size, the cut conductive foils being carried to each process.

[0079] Subsequently, there are a step of removing the first conductive foil 60A, except for at least a region which becomes the first conductive paths 51A to 51C, a step of mounting the circuit elements 52 on the first conductive path 60A, and a step of coating the insulating resin 50 in a trench 61 and the laminated conductive foil 60 to seal the circuit elements.

[0080] Firstly, a photo-resist (PR) (etching resistant mask) is applied on the first conductive foil 60A of the Cu foil 60, and patterned to expose the first conductive foil 60A excluding the region which becomes the first conductive paths 51A to 51C, as shown in Fig. 4. And etching is performed via the photo-resist PR, as shown in Fig. 5A.

[0081] This manufacturing method has a feature that the wet etching or dry etching is performed isotropically, the lateral face being a rough face and curved.

[0082] In the wet etching, etchant may be ferric chloride or cupric chloride. The conductive foil may be dipped in this etchant, or this etchant may be showered. Herein, the wet etching is typically made isotropically, so that the lateral face has the curved structure. When ferric chloride is used as the etchant, Al does not act as an etching stopper, because Al has a higher etching rate than Cu. Therefore, when the first conductive foil 60A is patterned as the first conductive paths 51A to 51C, the thickness of the second conductive foil 60B is needed to be increased, so that the second conductive foil 60B of Al can support integrally this first conductive paths 51A to 51C. In this case, as shown by dotted line, trench is formed in not only the first conductive foil 60A but also the second conductive foil 60B.

[0083] In the dry etching, the anisotropic etching or isotropic etching can be made. At present, it is said that Cu can not be removed by reactive ion etching. Cu can be removed by sputtering. The anisotropic etching or isotropic etching can be effected, depending on the sputtering or etching conditions . The lateral face of the trench 61 has the curved structure by etching isotropically.

[0084] Herein, it is preferable to use an etchant in which Cu is etched and Al is not etched, and in which Al acts as etching stopper.

[0085] Particularly as shown in Fig. 5B, etching in the transversal direction is difficult to proceed directly under the photo-resist PR as the etching mask, but is gradually made in a deeper portion of the photo-resist PR in the transversal direction. As shown in the figure, with reference to a certain position on the lateral face of the trench 61, the size of aperture corresponding to its position is smaller with increased height, to taper inversely, resulting in the anchor structure. By showering, the etching proceeds in the depth direction, but is suppressed in the transversal direction, so that this anchor structure becomes remarkable.

[0086] In Fig. 4, a conductive material which is resistant to the etching liquid may be selectively coated, instead of the photo-resist. By coating selectively this conductive material on a portion serving as the conductive path, this conductive material becomes an etching protective film, so that the trench can be etched without the use of the resist. The conductive materials may include Ni, Ag, Au, Pt and Pd. These corrosion resistant conductive materials have a feature of being readily available as the die pad or bonding pad.

[0087] For example, Ag can be bonded with Au and the brazing material. Hence, if Au has been coated on the back face of chip, the thermocompression bonding of chip can be effected with the Ag on the conductive coat 51, or the chip can be fixed via the brazing material such as solder. Since the Ag bonding wire can be bonded to the conductive coat of Ag, the wire bonding is allowed. Accordingly, there is provided a merit that these

conductive coats can be directly utilized as the die pad and the bonding pad.

[0088] Subsequently, there is a step of connecting electrically the circuit elements 52A, 52B to the first conductive paths 51A to 51C formed with the trench 61, as shown in Fig. 6.

[0089] The circuit elements 52 include the semiconductor device 52A such as a transistor, a diode and an IC chip, and the passive element 52B such as a chip capacitor and a chip resistor. These elements maybe bare chips or sealed chips. Though being thick, a face down element (also referred to as a flip chip) such as CSP or BGA can be mounted.

[0090] Herein, the bare transistor chip 52A is die bonded to the first conductive path 51A. Also, the emitter electrode and the first conductive path 51B, as well the base electrode and the first conductive path 51B, are connected via the bonding wire 55A which has been fixed by ball bonding with thermocompression, or wedge bonding with ultrasonic wave. The chip capacitor or the passive element is mounted between the first conductive paths 51B and 51C via the brazing material such as solder or the conductive paste 55B such as Ag paste.

[0091] When the pattern of Fig. 28 is applied in this embodiment, the bonding pad 26, which is small in size, is provided integrally with the second conductive foil 60B, as shown in Fig. 5. Hence, there is a merit that the energy of bonding tool can be transferred, with greater bonding ability. In cutting the bonding wire after bonding, the bonding wire maybe pull-cut. Then, since the bonding pad is integrated with the second conductive foil 60B, floating of the bonding pad can be suppressed, leading to better pull-cut ability.

[0092] Further, there is a step of attaching the insulating resin 50 onto the first conductive paths 51A to 51C and the curved trench 61, as shown in Fig. 7. This can be performed by transfer molding, injection molding, dipping or application. The resin materials include a thermosetting resin such as epoxy resin for which the transfer molding is suitable, and a thermoplastic resin such as polyimide resin and polyphenylene sulfide for which the injection molding is usable.

[0093] In this embodiment, the insulating resin 50 applied on the surface of the conductive foil 60 is adjusted so as to cover the thickness of about 100μm from the top portion of the circuit element (top of the bonding wire 55A). This thickness may be increased or decreased in consideration of the strength.

[0094] The second conductive foil 60B which is held in the sheet state is not divided like the first conductive paths 51A to 51C. Accordingly, it can be treated integrally as one sheet laminated conductive foil 60. It has a feature of the easy operation of carrying or mounting it onto the mold, when molding the insulating resin.

[0095] Further, since the insulating resin 50 is fitted into the trench 61 having the curved structure, there occurs the anchor effect in this region to prevent the insulating resin 50 from being peeled, and the conductive paths 51 from slipping off the insulating resin 50, the conductive paths 51 being separated at the later step.

[0096] Before coating this insulating resin 50, the silicone resin may be potted to protect the semiconductor chip or bonding wire, for example.

[0097] Subsequently, there is a step of removing chemically and/or physically the back face of the second conductive foil 60B for separation into the conductive paths 51. This step of removing can be effected by polishing, grinding, etching, or metal evaporation with laser.

[0098] Herein, an alkali solution of sodium hydroxide is used for etching. The sodium hydroxide can etch Al but not CU, and therefore does not etch the first conductive paths 51A to 51C.

[0099] As a result, the second conductive paths 51S to 51U are exposed from the insulating resin 50. And the bottom of the trench 61 is exposed, resulting in the trench 54 as shown in Fig. 1. The entire second conductive foil 60B may be removed (see Fig. 7).

[0100] Lastly, a conductive material such as solder may be applied onto the second conductive paths 51S to 51U exposed, as required, to complete the circuit device as shown in Fig. 1.

[0101] In the case where the conductive material is coated on the back face of the conductive paths 51S to 51U, the conductive coat may be formed ahead on the back face of the conductive foil of Fig. 3. In this case, the conductive coat may be selectively applied on the portion corresponding to the conductive path. The way of coating may be by plating. This conductive coat may be a material resistant to etching.

[0102] With this manufacturing method, the transistor and the chip resistor are only mounted on the conductive paths, but may be arranged in a matrix of transistors and chip resistors, or a matrix of circuits as shown in Fig. 28. In this case, the matrix can be divided into individual units by using a dicing apparatus, as will be described later.

[0103] With this manufacturing method, the circuit device 53 can be fabricated in which the first conductive paths 51A to 51C are buried into the insulating resin 50, and the second conductive paths 51S to 51U are exposed on the back face of the insulating resin 50.

[0104] The insulating resin 50 is required to have the conductive paths 51 buried therein. There is no need of having unnecessary support substrate 5, unlike the conventional manufacturing method of Fig. 6. Accordingly, it can be manufactured with the minimum amount of material, with less cost (see Fig. 1).

Second embodiment for a manufacturing method of a circuit device

[0105] Referring to Figs . 3 to 7 and Fig. 1 again, a manufacturing method of the circuit device 53 will be described below. This second embodiment is different from the previous embodiment in that the first conductive foil 60A is made of Al, and the second conductive

foil 60B is made of Cu. Each of the steps is substantially the same. Accordingly, only the different points will be detailed below, and other points omitted.

[0106] This laminated conductive foil 60 may be made by laying a Cu thin film on an Al foil, or an Al thin film on a Cu foil, as described in the previous embodiment. This thin film may be made by plating, deposition, or sputtering, or prepared in a state of foil, and laminated and bonded under pressure (see Fig. 3).

[0107] Subsequently, the photo-resist PR is formed on the laminated conductive foil 60, and is left on the portions corresponding to the conductive paths (see Fig. 4).

[0108] Subsequently, the first conductive foil 60A is patterned via the photo-resist PR. In this step, an alkali solution such as sodium hydroxide is used as etchant. This sodium hydroxide etches Al but does not etch Cu. Therefore, there is no need of considering the thickness of the second conductive foil, like the previous embodiment. Accordingly, the second conductive foil 60B made of Cu can be made thinner or thicker. Due to wet etching, the lateral face is curved. If the showering is performed, it is further curved. Using a C12 gas or a mixture of BC13 and C12 gases, dry etching can be effected isotropically (see Fig. 5).

[0109] Subsequently, there is a step of mounting the circuit elements 52. Herein, if an Ag paste is applied and sintered on the surface of the first conductive paths 51A to 51C, the circuit elements can be joined with Au on the back face of the semiconductor chip. The bonding wire 55A made of Al or Au can be bonded. Ag is superior in the adhesiveness with the brazing material such as solder, and fixed via the brazing material 55B (see Fig. 6).

[0110] Subsequently, there is a step of applying the insulating resin 50. This step is exactly the same as in the previous embodiment, and not described.

[0111] Subsequently, there is a step of patterning the second conductive foil 60B. The photo-resist PR is patterned so that the portion corresponding to the second conductive path may be left. Etching is performed using an etchant such as ferric chloride, cupric chloride or sodium hydroxide. Preferably, Cu is etched, but Al is not etched by etchant (see Fig. 7).

[0112] Lastly, a conductive material such as solder is applied on the second conductive paths 51S to 51U exposed, as required. Consequently, the circuit device as shown in Fig. 1 is completed.

[0113] Ag may be used for this conductive material. In this case, Ag may be plated entirely on the back face of the second conductive foil 60B of Fig. 3, or partly plated. Ultimately, Ag provided on the back face of the second conductive paths 51S to 51U and the Cu wire on the mounting substrate can be fixed via the brazing material.

[0114] With this manufacturing method, when the first conductive foil 60A made of Ag is etched in the first conductive paths 51A to 51C, its lateral face can be curved, resulting in the anchor effect. Hence, it is possible to prevent the conductive paths from slipping.

Third embodiment for a manufacturing method of a circuit device

[0115] Referring to Figs. 9 to 13 and Fig. 8, a manufacturing method of a circuit device 56 having a visor will be described below. The third embodiment is substantially the same as the first embodiment (Figs. 1 and 2), except that a conductive material 70 (hereinafter referred to as a second material) which serves as the visor is applied. The details are not described here.

[0116] Firstly, a laminated conductive foil 60 is prepared in which the second material 70 having a small etching rate is applied on the first conductive foil 60A made of the first material, as shown in Fig. 9.

[0117] For example, if Ni is applied on the Cu foil, Cu and Ni can be etched by ferric chloride or cupric chloride at a time, advantageously resulting in the formation of the visor 58 of Ni, due to a difference between etching rates. The bold line indicates the conductive coat 70 made of Ni, its film thickness being preferably about 1 to 10μm. The larger film thickness of Ni can form the visor 58 more easily.

[0118] The second material may cover the first material as well as the material for selective etching. In this case, the film made of the second material is firstly patterned to cover the formed area of the first conductive paths 51A to 51C. Then, with this film as a mask, the first conductive path 60A made of the first material is etched so that the visor 58 can be formed. The second materials may include Al, Ag and Au (see Fig. 9).

[0119] Subsequently, there is a step of removing the first conductive foil 60A except for at least the region which becomes the first conductive paths 51A to 51C.

[0120] The photo-resist PR is formed on the Ni conductive coat 70, and patterned so that the Ni conductive coat 70 may be exposed except for the region which becomes the first conductive paths 51A to 51C, as shown in Fig. 10. Then, etching is performed with the photo-resist, as shown in Fig. 11.

[0121] As described previously, if etching is performed, using an etchant such as ferric chloride or cupric chloride, the visor 58 juts out as the etching proceeds, because the Ni conductive coat 70 has a slower etching rate than the conductive foil Cu 60.

[0122] The steps of mounting the circuit elements 52 in the first conductive paths 51A to 51C with the trench 61 formed (Fig. 12), covering the insulating resin 50 over the first conductive foils 51A to 51C and the trench 61, removing the second conductive foil 60B chemically and/or physically for separation into the second conductive paths 51S to 51U (Fig. 13), and forming the conductive coat on the back face of the conductive paths to complete the circuit device (Fig. 8) are the same as those of the previous manufacturing method, and not described again.

[0123] The double anchor effect is produced by the

visor 58 and the curved structure 59, and can prevent slippage and curvature of the conductive paths.

Fourth embodiment for a manufacturing method of a circuit device

[0124] Referring to Figs. 14 to 20, a method for manufacturing a circuit device will be described below, in which the IC circuits having the conductive paths composed of a plurality of kinds of circuit elements, wires, die pads and bonding pads are arranged like a matrix and divided into individual IC circuits after sealing. Referring to Fig. 2 and particularly a cross-sectional view of Fig. 2C, the structure will be described below. This manufacturing method is substantially the same as in the first embodiment and the second embodiment, and is simply described.

[0125] Firstly, the sheet laminated conductive foil 60 is prepared, as shown in Fig. 14.

[0126] The second conductive foil 60B is required to be thick enough to support the first conductive paths not to break off, when forming the trench 61 at the step of Fig. 16. Herein, one is Al, and the other is Cu. Laying order is out of consideration. The sheet laminated conductive foil 60 is rolled in a predetermined width, and may be carried to the later process. Or the conductive foils cut in a predetermined size may be prepared and carried to the later process.

[0127] Subsequently, there is a step of removing the first conductive foil 60A except for at least the region which becomes the first conductive paths 51A to 51C.

[0128] Firstly, the photo-resist PR is made on the first conductive foil 60A, and patterned so that the first conductive foil 60A may be exposed except for the region which becomes the first conductive paths 51A to 51C, as shown in Fig. 15. And etching is performed via the photo-resist PR, as shown in Fig. 6.

[0129] The lateral face of the trench 61 formed by etching is rough, leading to increased adhesiveness of the insulating resin 50.

[0130] The lateral face of the trench 61 is etched isotropically, and curved. This step of removing can be wet etching, or dry etching. This curved structure produces the anchor effect. (For more details, refer to the first embodiment for the manufacturing method of the circuit device.)

[0131] In Fig. 15, a conductive material which is resistant to the etching solution may be selectively coated, instead of the photo-resist PR. If it is selectively coated on the portion for the first conductive paths, this conductive material serves as an etching protective film. As a result, the trench can be etched without the use of resist.

[0132] Subsequently, there is a step of electrically connecting and mounting the circuit elements 52A to the first conductive foil 60A formed with the trench 61, as shown in Fig. 17.

[0133] The circuit elements 52A include semiconductor devices such as a transistor, a diode, and an IC chip, and passive elements such as a chip capacitor and a chip resistor. Also, though being thicker, the face down semiconductor devices (flip chip) such as CSP and BGA may be mounted.

[0134] Herein, the bare transistor chip 52A is die bonded to the conductive path 51A. Consequently, the emitter electrode and the first conductive path 51B, as well as the base electrode and the conductive path 51B are connected via the bonding wire 55A.

[0135] Furthermore, there is a step of attaching the insulating resin 50 to the laminated conductive foil 60 and the trench 61, as shown in Fig. 18. This step can be performed by transfer molding, injection mold, dipping or application.

[0136] In this embodiment, the insulating resin applied on the surface of the laminated conductive foil 60 is adjusted to be about 100μm thick from the top of the circuit elements. This thickness can be made thicker or thinner in view of the strength.

[0137] With the trench 61, the conductive foil 60A is not divided into the first conductive paths 51A to 51C, because the second conductive foil 60B is left behind like a sheet. Accordingly, this embodiment has a feature that the sheet laminated conductive foil 60 can be singly handled, facilitating the operation of carrying and mounting it to the mold when molding the insulating resin.

[0138] Subsequently, there is a step of removing the back face of the second conductive foil 60B chemically and/or physically or separation into the conductive paths 51. Herein, the step of removing is performed by etching. As a result, the second conductive paths 51S to 51U are exposed on the back face of the insulating resin 50.

[0139] Further, a conductive material such as solder is applied on the exposed second conductive paths 51S to 51U, as shown in Fig. 19.

[0140] Lastly, there is a step of completing the circuit device by separation into individual circuit elements, as shown in Fig. 20.

[0141] The separation line is indicated by the arrow, and separation can be effected by dicing, cut, press, or chocolate break. When using the chocolate break, a projection on the mold may be provided to form the groove at the separation line in coating the insulating resin.

[0142] Particularly, the dicing is mostly used in the manufacturing method of the semiconductor devices, and is preferable because it can cut very small things.

[0143] The manufacturing method as described in the first to third embodiments allows for the complex patterns, as shown in Fig. 28. Particularly, the wire is bent and integral with the bonding pad 26, the other end being electrically connected with the circuit element. The wire is narrow in width, and long. Therefore, the curvature caused by heat is very significant, resulting in exfoliation in the conventional structure. However, in the present invention, since the wires are buried into the insulating resin and supported, it is possible to prevent

curvature, exfoliation and slippage of the wires. The bonding pad itself has a small plane area, and may be peeled in the conventional structure. However, since in the present invention, the bonding pad is buried into the insulating resin and supported by the insulating resin, with curved structure having the anchor effect, there is a merit of preventing the slippage.

[0144] Further, there is another merit that the circuit device having the circuit elements buried into the insulating resin 50 can be produced. This is similar to the conventional structure in which a circuit is incorporated into a printed circuit board or a ceramic substrate. This will be described later in connection with a way of mounting.

[0145] To the right of Fig. 27, a simple flow diagram of the present invention is presented. The circuit device can be fabricated in accordance with the nine steps of preparing the laminated conductive foil, plating with Ag or Ni, etching the first conductive foil, die bonding, wire bonding, transfer molding, etching the second conductive foil, treating the back face of conductive path, and dicing. And all the steps can be performed in the inside work without supplying the support substrate from the manufacturer.

Mode for providing various kinds of circuit devices and the ways of mounting

[0146] Fig. 21 shows a circuit device 81 having a face down circuit element 80 mounted. The circuit element 80 is a bare semiconductor chip, CSP or BGA (flip chip) having sealed surface. Fig. 22 shows a circuit device 83 having a passive element 82 such as a chip resistor mounted. Since they are of thin type, and sealed by the insulating resin, they are superior in the environmental resistance.

[0147] Fig. 23 shows the mounting structure. Firstly, Fig. 23A shows the circuit devices 53, 56, 81, 83 as described above, which are mounted in the conductive paths 85 formed on a mounting substrate 84 such as a printed circuit board, metal substrate, or ceramic substrate.

[0148] Particularly, a conductive path 51A to which the back face of a semiconductor chip 52 is fixed is thermally coupled to the conductive paths 85 on the mounting substrate 84. Therefore, the heat of the circuit device can be radiated via the conductive paths. If the metal substrate is used for the mounting substrate 84, the temperature of the semiconductor chip 52 can be further decreased, due to radiation of the metal substrate. Therefore, the driving capability of the semiconductor chip can be enhanced.

[0149] For example, the power MOS, IGBT, SIT, large current driving transistors, and large current driving IC (MOS, BIP, Bi-CMOS) memory elements are preferable.

[0150] The metal substrates preferably include an Al substrate, a Cu substrate and a Fe substrate. In view of the short-circuit with the conductive paths 85, the insulating resin and/or oxide films are formed.

[0151] Fig. 23B shows a circuit device 90 of the invention which is utilized as the substrate of Fig. 23A. This is the greatest feature of the present invention. Namely, the conventional printed circuit board or ceramic substrate has a through hole TH formed in the substrate. In the present invention, a substrate module containing an IC circuit can be fabricated. For example, at least one circuit (which may be contained as the system) is contained in the printed circuit board.

[0152] Conventionally, the support substrate used the printed circuit board or ceramic substrate. In the present invention, the substrate module does not need the support substrate. This substrate module can be thinner and lighter than a hybrid substrate which may be the printed circuit board, the ceramic substrate, or the metal substrate.

[0153] This circuit device 90 is utilized as the support substrate, and the circuit elements can be mounted in the exposed conductive paths, resulting in a high performance substrate module. Particularly, if this circuit device is a support substrate and a circuit device 91 is mounted on the support substrate, the substrate module can be made further thinner and lighter.

[0154] Accordingly, according to the above embodiments, an electronic apparatus with this module mounted can be reduced in size and weight.

[0155] The hatching part indicated by numeral 93 is an insulating film. For example, a high molecular film such as solder resist is preferable. Due to formation of this film, it is possible to prevent the conductive paths buried into the substrate 90 and the electrodes formed on the circuit elements 91 from short-circuiting.

[0156] Referring to Fig. 29, there will be described some merits of the present circuit device in the following. In the conventional mounting method, the semiconductor manufacturers fabricated the package type semiconductor devices and flip chips. The set makers mounted the semiconductor devices supplied from the semiconductor manufacturers and the passive elements supplied from the parts makers on the printed circuit board and incorporated the circuit devices into the set to fabricate an electronic apparatus. However, since the circuit device of this invention allows itself to be used as the mounting substrate, the semiconductor manufacturers can complete the mounting substrate module in the later process, and deliver it to the set makers. Accordingly, the set makers can greatly save the operation of mounting the elements on the substrate.

[0157] As will be clearly understood, the present invention can fabricate the circuit devices with the conductive paths and the minimum amount of insulating resin, resulting in less wasteful resources. Hence, the circuit devices can be fabricated with less superfluous components up to completion, and with greatly reduced cost. The film thickness of insulating resin, and the thickness of conductive foil, can be optimized, to make the circuit device smaller, thinner and lighter. Furthermore,

since the wires liable to curvature or exfoliation are buried into the insulating resin, those problems can be resolved.

[0158] Since the back face of conductive paths is exposed from the insulating resin, the back face of conductive paths can be directly contacted with the external. Hence, there is an advantage that the back face electrode and through hole of the conventional structure can be dispensed with.

[0159] When the circuit elements are directly fixed via the conductive coat made of the brazing material, Au or Ag, the heat developed by the circuit elements can be transferred directly via the conductive paths to the mounting substrate, because the back face of conductive paths is exposed. Particularly, the power elements can be also mounted, due to this heat radiation.

[0160] Since the conductive paths has the curved structure on the lateral face, and/or the second material is formed on the surface of conductive paths, a visor applied to a conductive path can be formed, bringing about the anchor effect to prevent the conductive paths from warping and slipping.

[0161] In the manufacturing method of the circuit device according to the present invention, the conductive foil itself serving as the conductive paths is utilized as the support substrate. The whole substrate is supported by the conductive foil, up to the steps of forming the trench or mounting the circuit elements and applying the insulating resin, while to divide the conductive foil into the conductive paths, the insulating resin is used as the support substrate. Accordingly, the circuit device of the invention can be manufactured with the least amount of circuit elements, conductive foil, and insulating resin, as required. As described in the conventional example, this circuit device can be fabricated without need of having the support substrate and with the reduced cost. Since the support substrate is unnecessary, the conductive paths are buried into the insulating resin, with the adjustable thickness of the insulating resin and the conductive foil, there is a merit that the circuit device can be made very thin. In forming the trench, the curved structure results, bringing about the anchor effect.

[0162] As will be apparent from Fig. 27, the steps of forming the through hole and printing the conductors (for the ceramic substrate) can be omitted. Therefore, the manufacturing process can be significantly shortened, and advantageously the whole process can be performed in the inside work. Also, the frame mold is unnecessary at all, leading to quite short delivery.

[0163] Since the conductive paths can be treated integrally, there is an advantage of the enhanced workability in the later step of coating the insulating resin.

[0164] Lastly, this circuit device can be utilized as the support substrate to mount the circuit elements in the exposed conductive paths, resulting in a substrate module with high performance. Particularly, if this circuit device is used as the support substrate and the circuit device 91 as the circuit element is mounted thereon, the substrate module can be made lighter and thinner.

Claims

1. A method for manufacturing a circuit device, comprising the steps of:

   forming a conductive path patterned in a predetermined shape by patterning a surface layer of a plate,
   electrically connecting a desired circuit element with said desired conductive path,
   coating said circuit element and said conductive path with an insulating resin, and
   exposing said conductive path by removing said plate from an opposite surface of the conductive path.

2. A method for manufacturing a circuit device, according to claim 1, wherein the step of forming a conductive path comprises a step of patterning so that a lateral face of the conductive pattern is curved.

3. A method for manufacturing a circuit device, according to claim 1, wherein the plate is made of copper foil.

4. A method for manufacturing a circuit device, according to claim 1,comprising the steps of:

   preparing a laminated conductive foil formed by laminating a second conductive foil on a first conductive foil,
   forming a conductive path patterned in a predetermined shape and having a curved lateral face with a conductive foil;
   electrically connecting and fixing a desired circuit element on said desired conductive path;
   coating said circuit element and said conductive path with an insulating resin; and
   removing said conductive foil excluding at least a portion corresponding to said conductive path.

5. Amethod for manufacturing a circuit device, according to claim 1, comprising the steps of:

   preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil;
   forming a first conductive path of curved structure on the lateral face by forming a trench in said first conductive foil excluding at least a region for the conductive path;
   electrically connecting and fixing a desired circuit element on said desired first conductive

path;
coating and molding said circuit element and said first conductive path with an insulating resin to be filled into said trench; and
removing said second conductive foil at a portion corresponding to said trench and forming a second conductive path on the back face of said first conductive path.

6. A method for manufacturing a circuit device, according to claim 1, comprising the steps of:

preparing a laminated conductive foil with a second conductive foil laminated on the back of a first conductive foil;
forming a corrosion resistant conductive coat on at least a region which becomes a conductive path on the surface of said first conductive foil;
forming a first conductive path of curved structure on the lateral face by forming a trench in said conductive foil excluding at least a region for the conductive path;
fixing a circuit element on said desired first conductive path;
forming connecting means for electrically connecting an electrode of said circuit element with said desired first conductive path;
coating and molding said circuit element, said connecting means and said first conductive path with an insulating resin to be filled into said trench, and fitting said conductive path and said insulating resin; and
removing said second conductive foil which is not provided with said trench, and forming a second conductive path on the back face of said first conductive path.

7. A method for manufacturing a circuit device according to claim 1, comprising the steps of:

preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil;
forming a conductive path of curved structure on the lateral face by forming a trench in said first conductive foil excluding at least a region for the conductive path;
fixing a circuit element on said desired conductive path;
forming connecting means for electrically connecting an electrode of said circuit element with said desired first conductive path;
coating and molding said circuit element, said connecting means and said first conductive path with an insulating resin to be filled into said trench, and fitting said first conductive path and said insulating resin; and
removing said first conductive foil which is not provided with said trench, and forming a second conductive path on the back face of said first conductive path.

8. A method for manufacturing a circuit device, according to claim 1, comprising the steps of:

preparing a laminated conductive foil with a second conductive foil laminated on the back face of a first conductive foil;
forming a corrosion resistant conductive coat in at least a region on said first conductive foil which becomes a conductive path;
forming a conductive path of curved structure on the lateral face by forming a trench in said first conductive foil excluding at least a region for the first conductive path;
fixing a circuit element on said desired first conductive path;
forming connecting means for electrically connecting an electrode of said circuit element with said desired first conductive path;
coating and molding said circuit element with an insulating resin to be filled into said trench, and fitting said first conductive path and said insulating resin;
removing said second conductive foil which is not provided with said trench, and forming a second conductive path on the back face of said first conductive path; and
severing said insulating resin for separation into individual circuit devices.

9. The method for manufacturing the circuit device according to any one of claims 4 to 8, wherein said second conductive foil is made of copper.

10. The method for manufacturing the circuit device according to any one of claims 4 to 8, wherein said second conductive foil is made of aluminum, or iron-nickel.

11. The method for manufacturing the circuit device according to any one of claims 4 to 10, wherein said first conductive foil is formed by plating.

12. The method for manufacturing the circuit device according to any one of claims 4 to 10, wherein said laminated conductive foil has a structure in which a conductive foil made of aluminum is plated with copper.

13. The method for manufacturing the circuit device according to any one of claims 4 to 10, wherein said first conductive foil is made of aluminum or copper.

14. The method for manufacturing the circuit device ac-

cording to claim 3 or 5, wherein said conductive coat is plated with nickel or silver.

15. The method for manufacturing the circuit device according to claim 5, wherein said trench selectively formed in said first conductive foil is made by chemical or physical etching.

16. The method for manufacturing the circuit device according to claim 5, wherein said conductive coat is used as part of a mask when forming said trench.

17. The method for manufacturing the circuit device according to any one of claims 4 to 16, wherein said circuit element is fixed with any one or two of a semiconductor bare chip, a flip chip, a chip circuit component, a package semiconductor element, and a CSP.

18. The method for manufacturing the circuit device according to any one of claims 4 to 17, wherein said connecting means is formed of wire bonding or brazing material.

19. The method for manufacturing the circuit device according to any one of the preceding claims, wherein said insulating resin is applied by transfer molding.

20. The method for manufacturing the circuit device according to any one of the preceding claims, further comprising separating into individual circuits by dicing.

21. The method for manufacturing the circuit device according to any one of the preceding claims, wherein said conductive path is at least the wire.

22. A circuit device comprising:

a conductive path patterned in a predetermined shape,
a circuit element connected with said desired conductive path, and
an insulating resin coating said circuit element and said conductive path so that at least of a part of the conductive path is exposed from the insulating resin.

23. A circuit device, according to claim 22, wherein a lateral face of the conductive pattern of the conductive path is curved.

FIG.1A

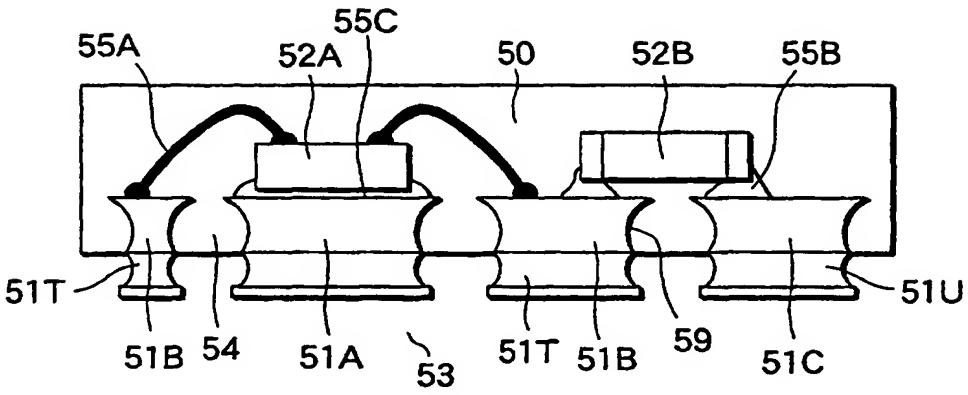

55A
55C
52A
50
52B
55B
51T
51U
51B
54
51A
53
51T
51B
59
51C

FIG.1B

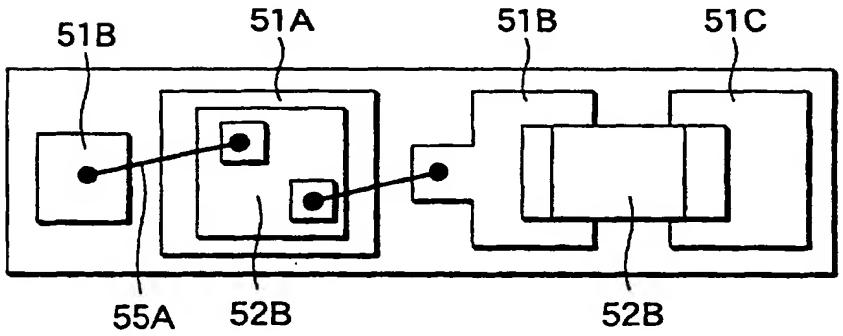

51B
51A
51B
51C
55A
52B
52B

FIG.2A

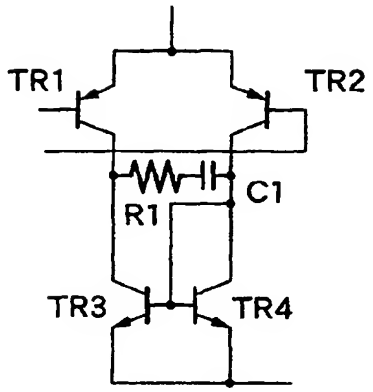


FIG.2B

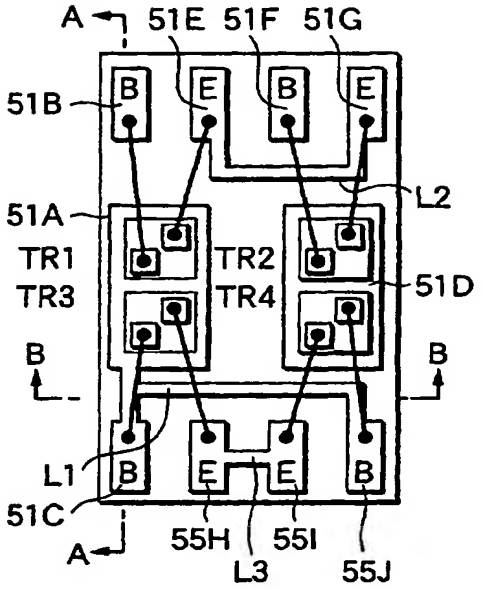


FIG.2C

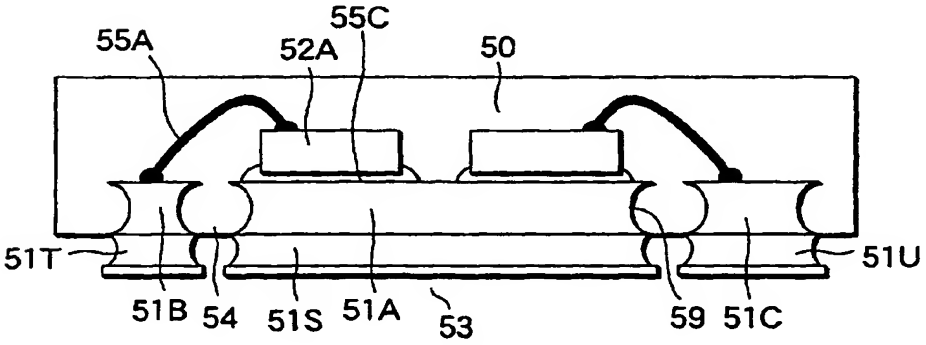


FIG.2D

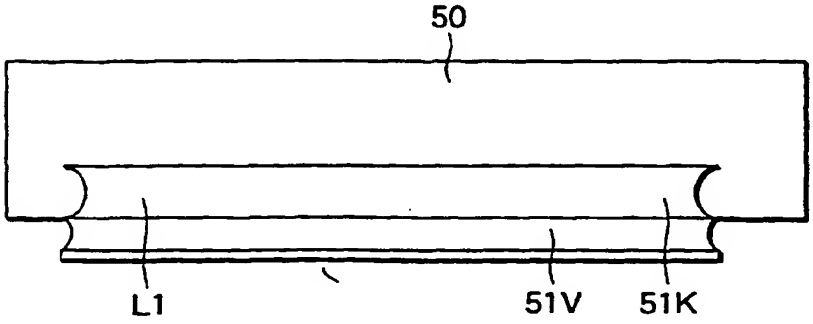


FIG.3

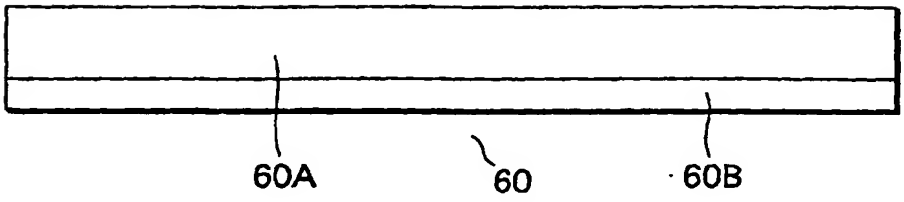


FIG.4

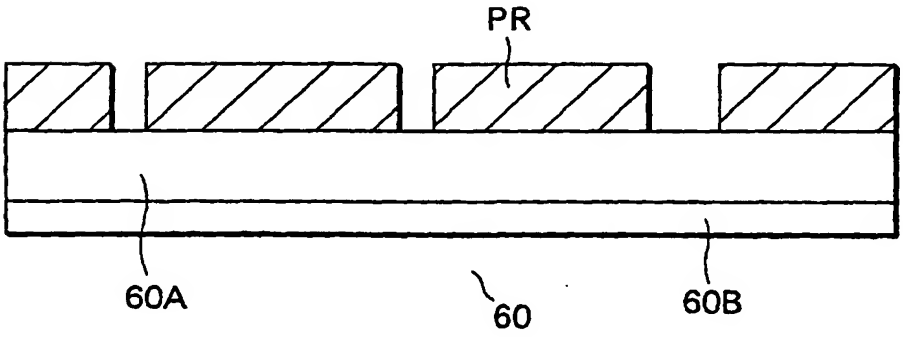


FIG.5A

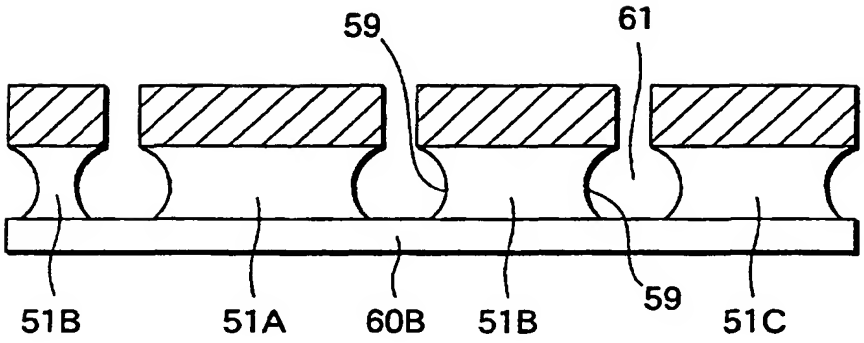


FIG.5B

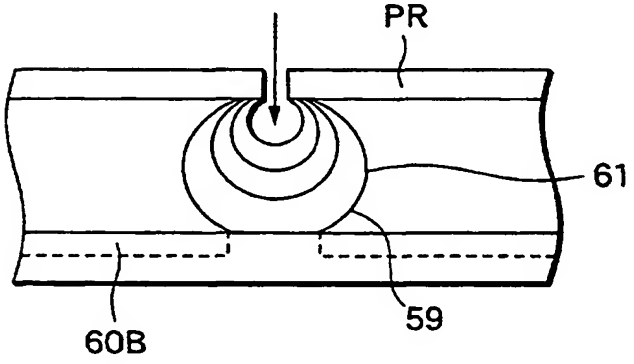
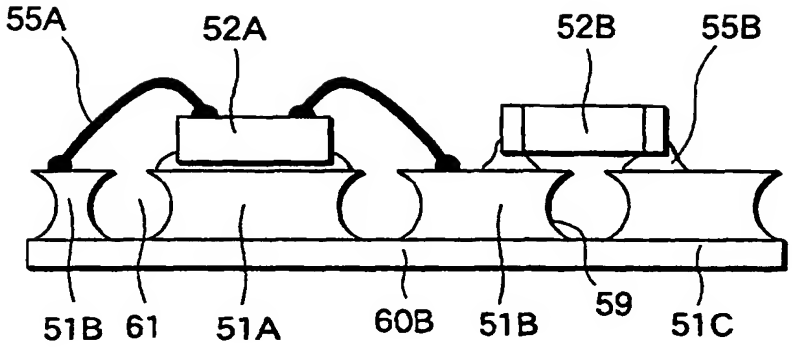


FIG.6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61
51A
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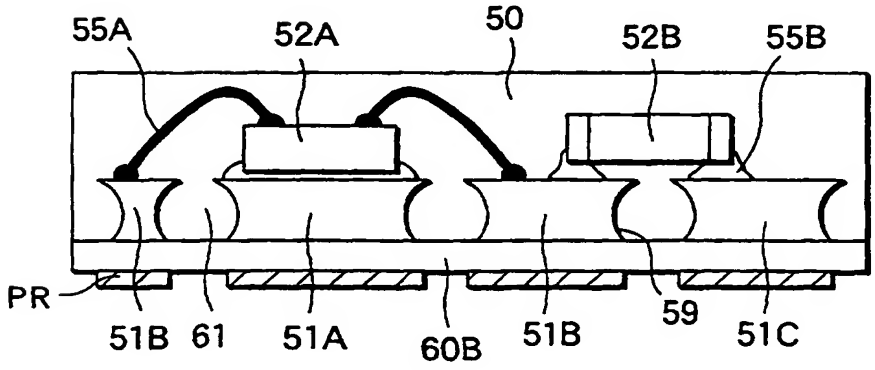
51B
59
51C

FIG.7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51C

FIG.8

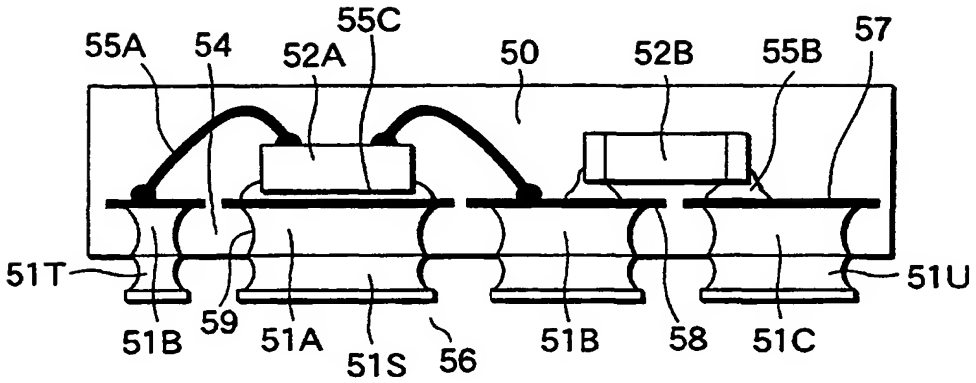

FIG.9

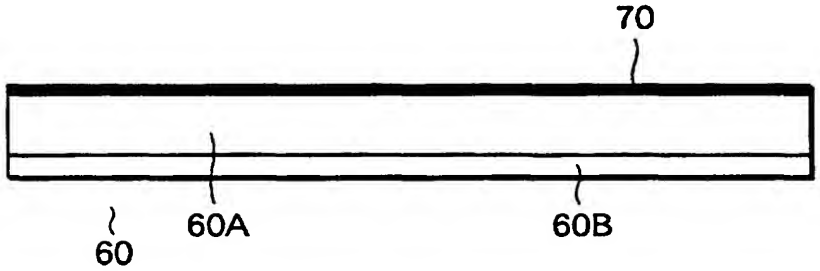

FIG.10

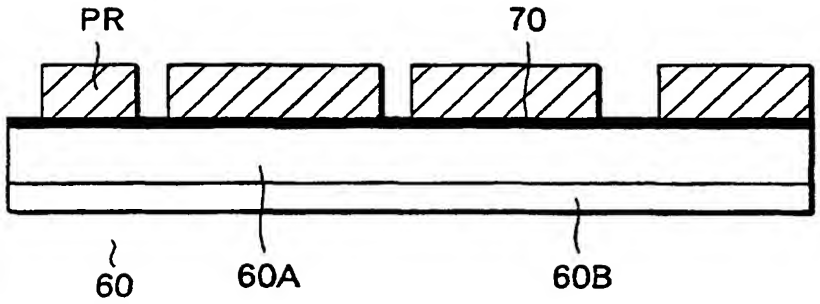

FIG.11

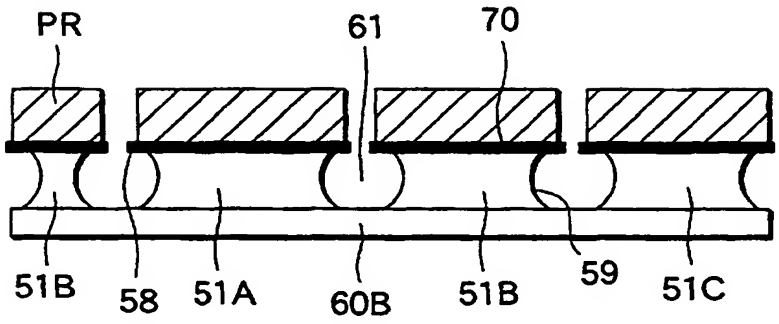
PR
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FIG.12

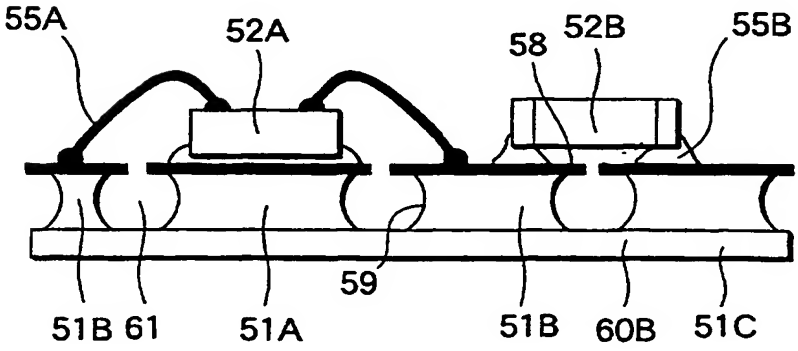
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FIG.13

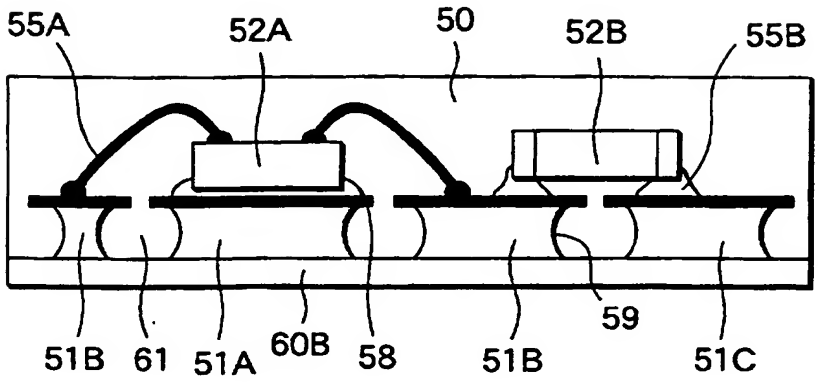

FIG.14

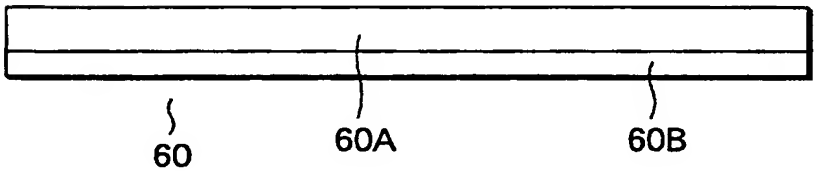

FIG.15

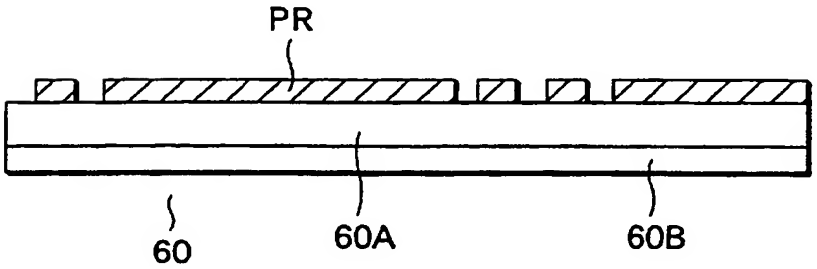

FIG.16

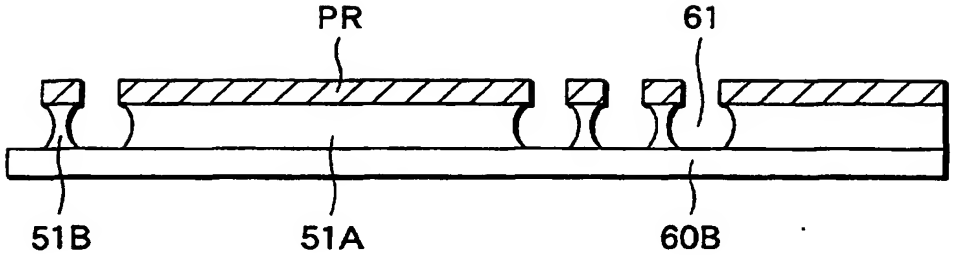

FIG.17

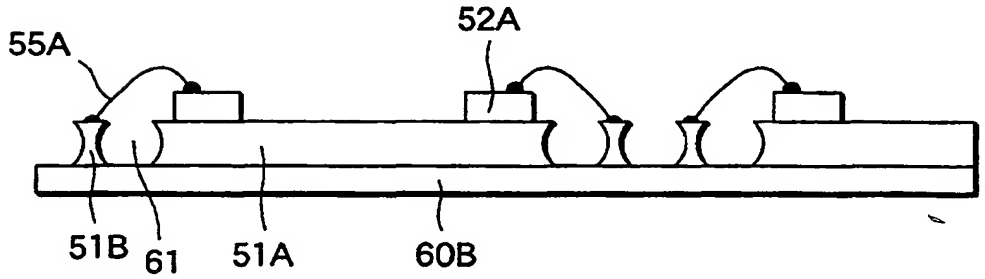

FIG.18

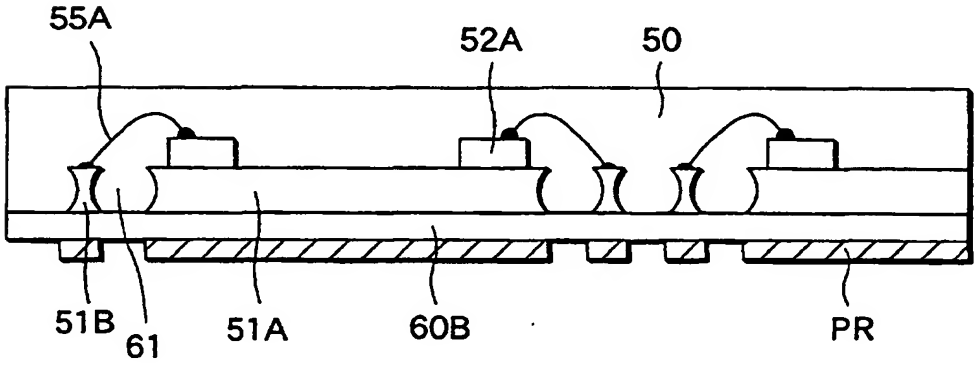

FIG.19

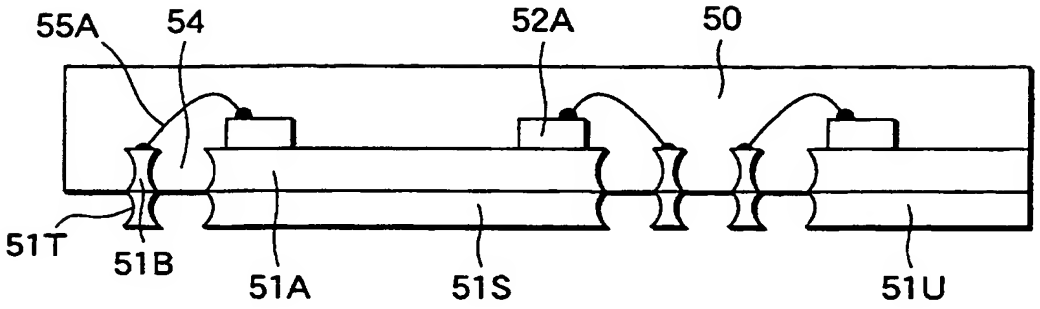

FIG.20

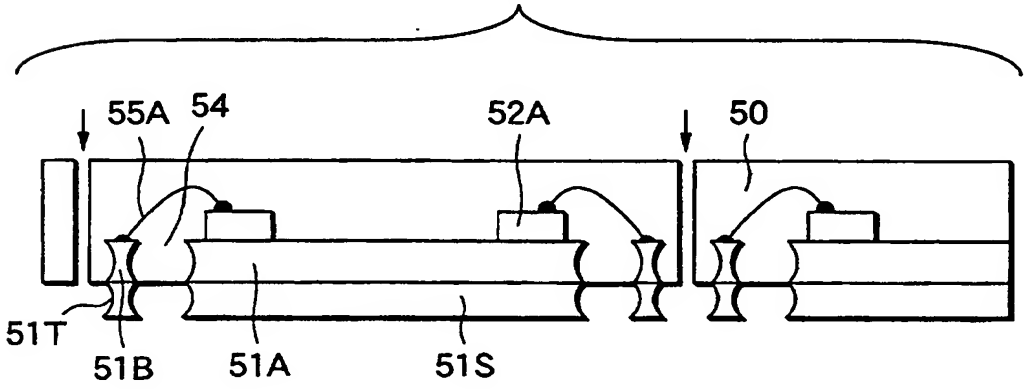

FIG.21

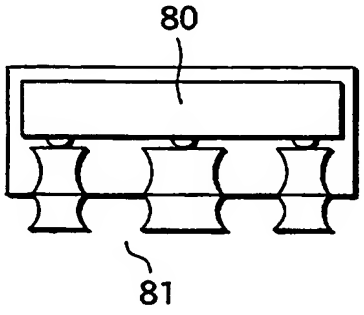

FIG.22

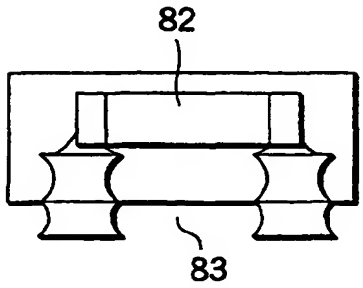

FIG.23A

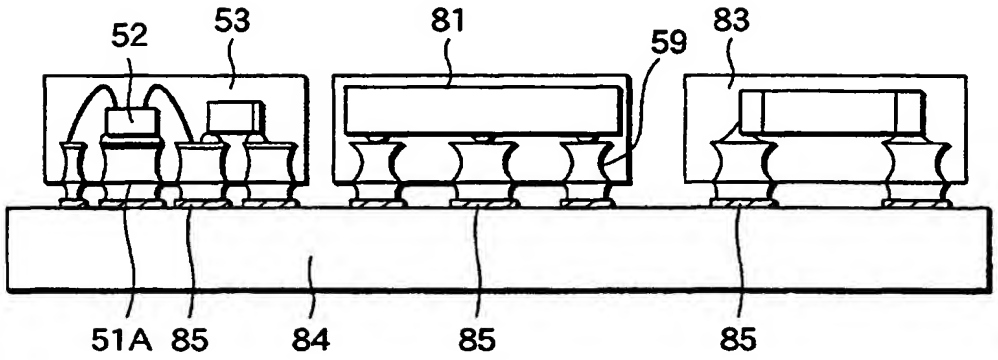

FIG.23B

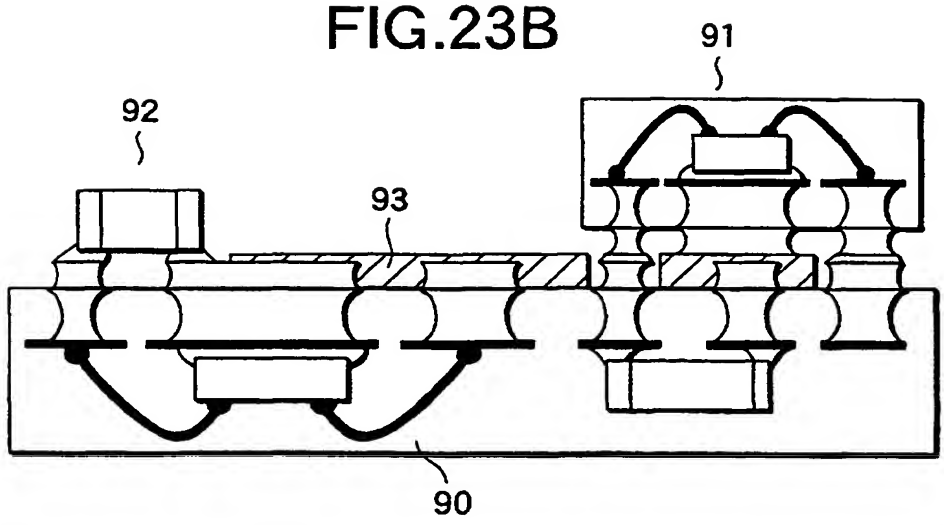

FIG.24

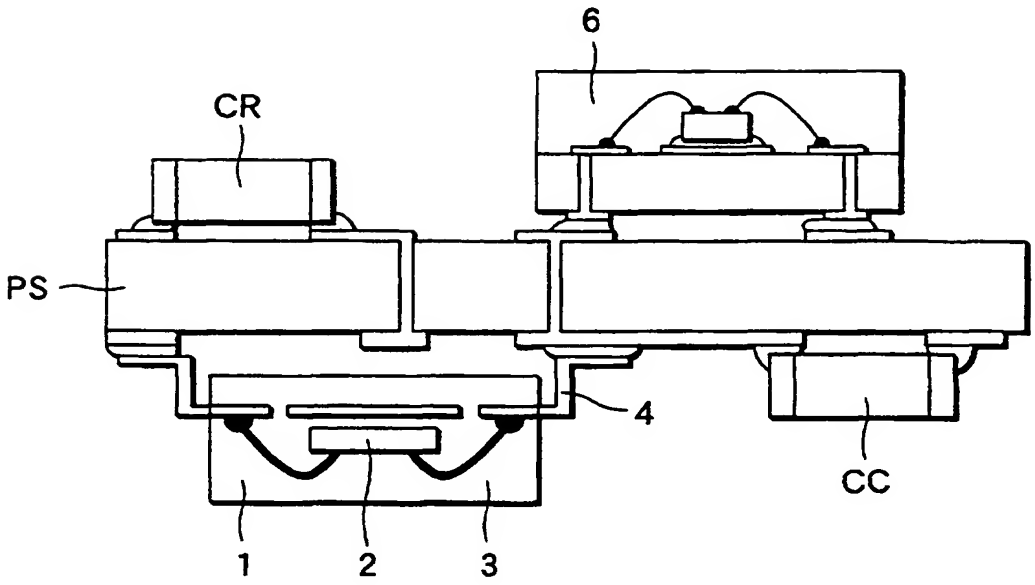

FIG.25

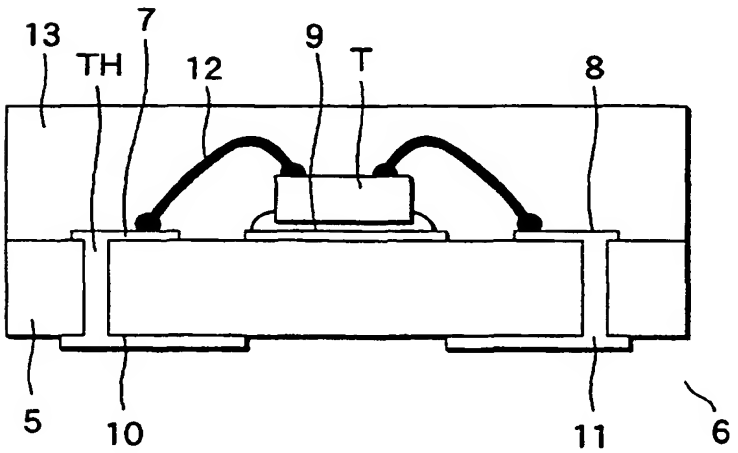

FIG.26A

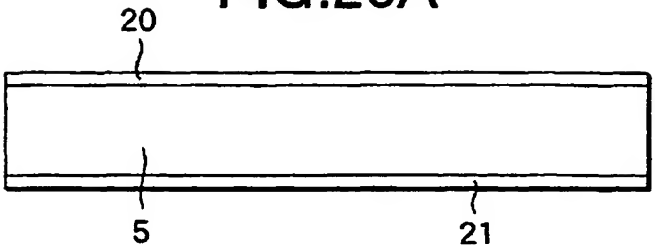

FIG.26B

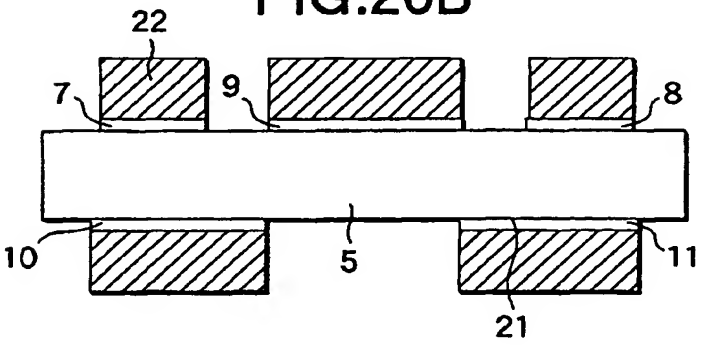

FIG.26C

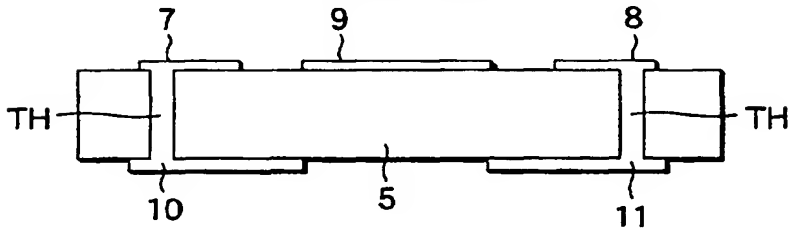

FIG.26D

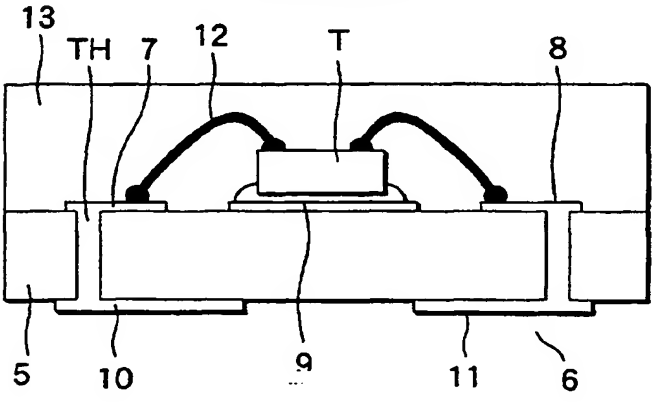

FIG.27

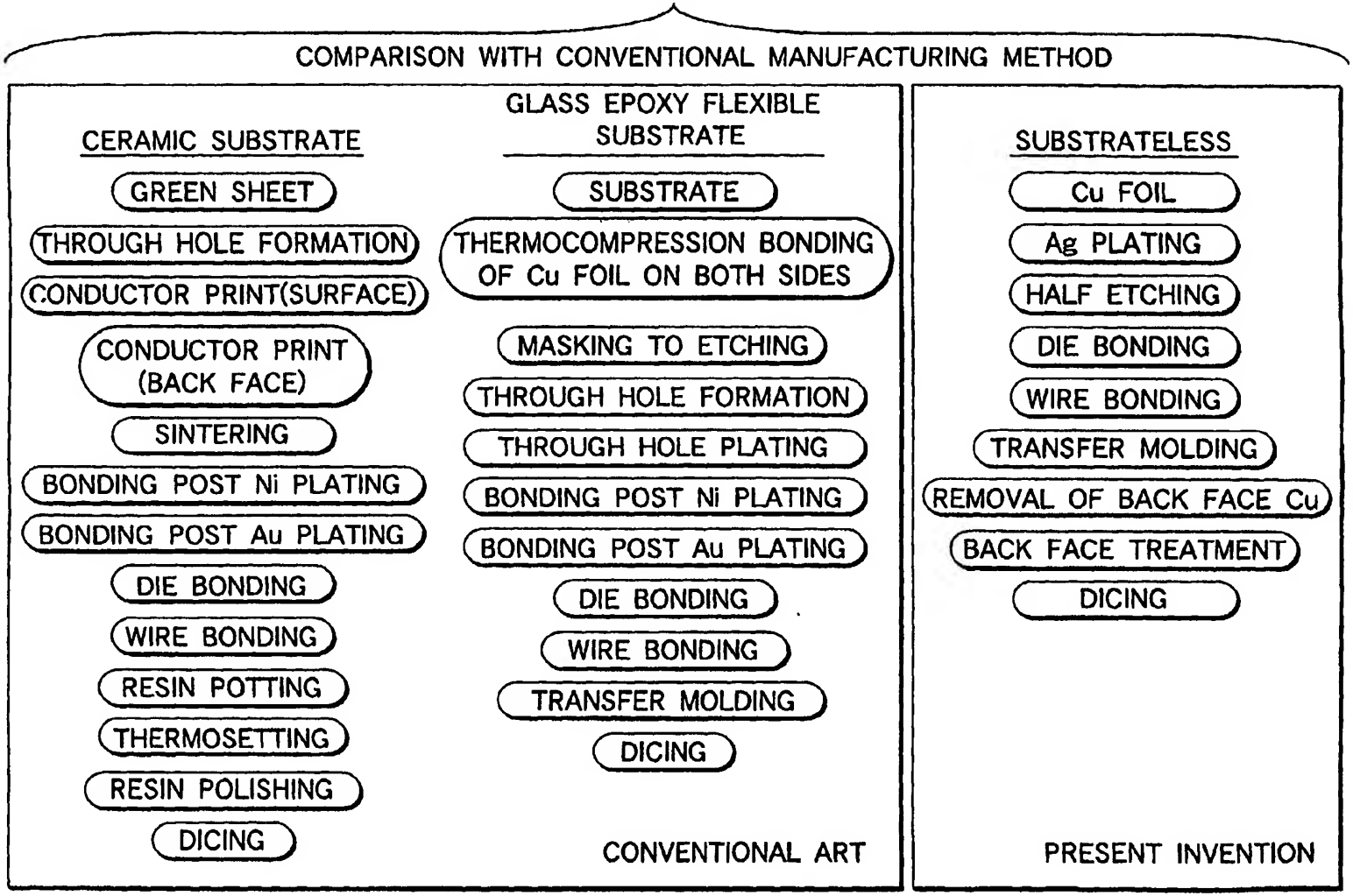

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FIG.28

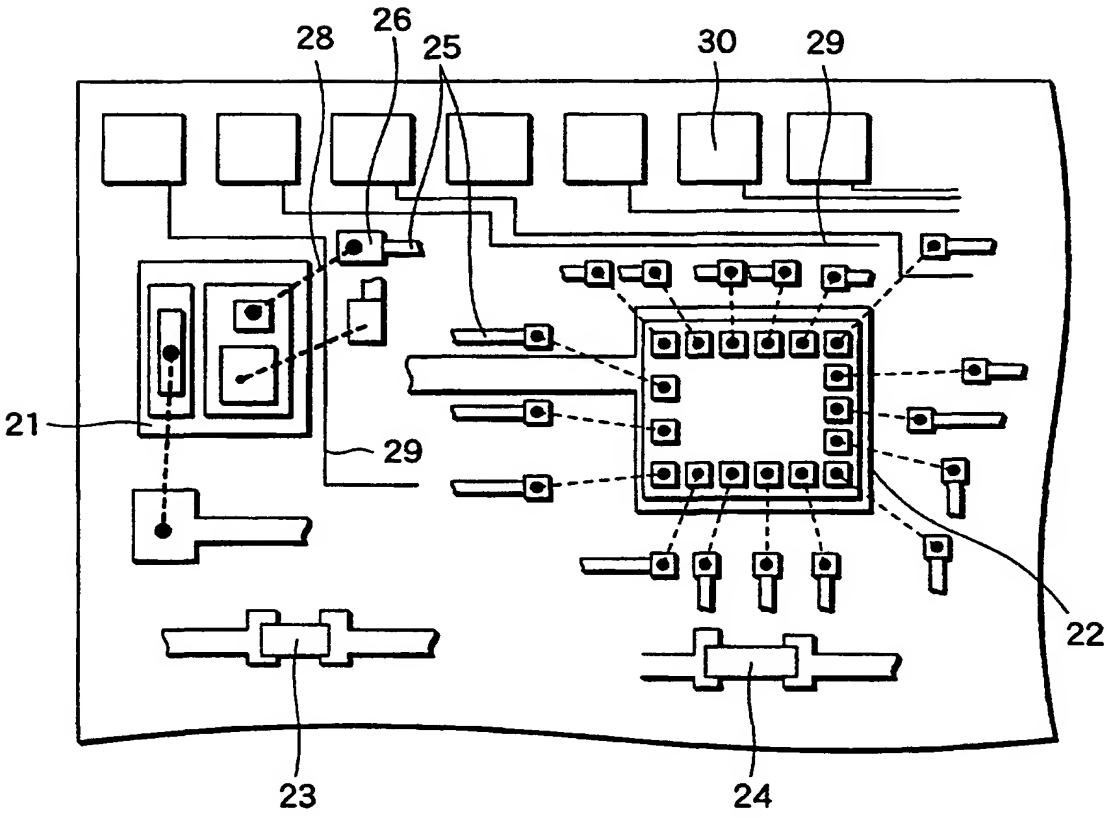
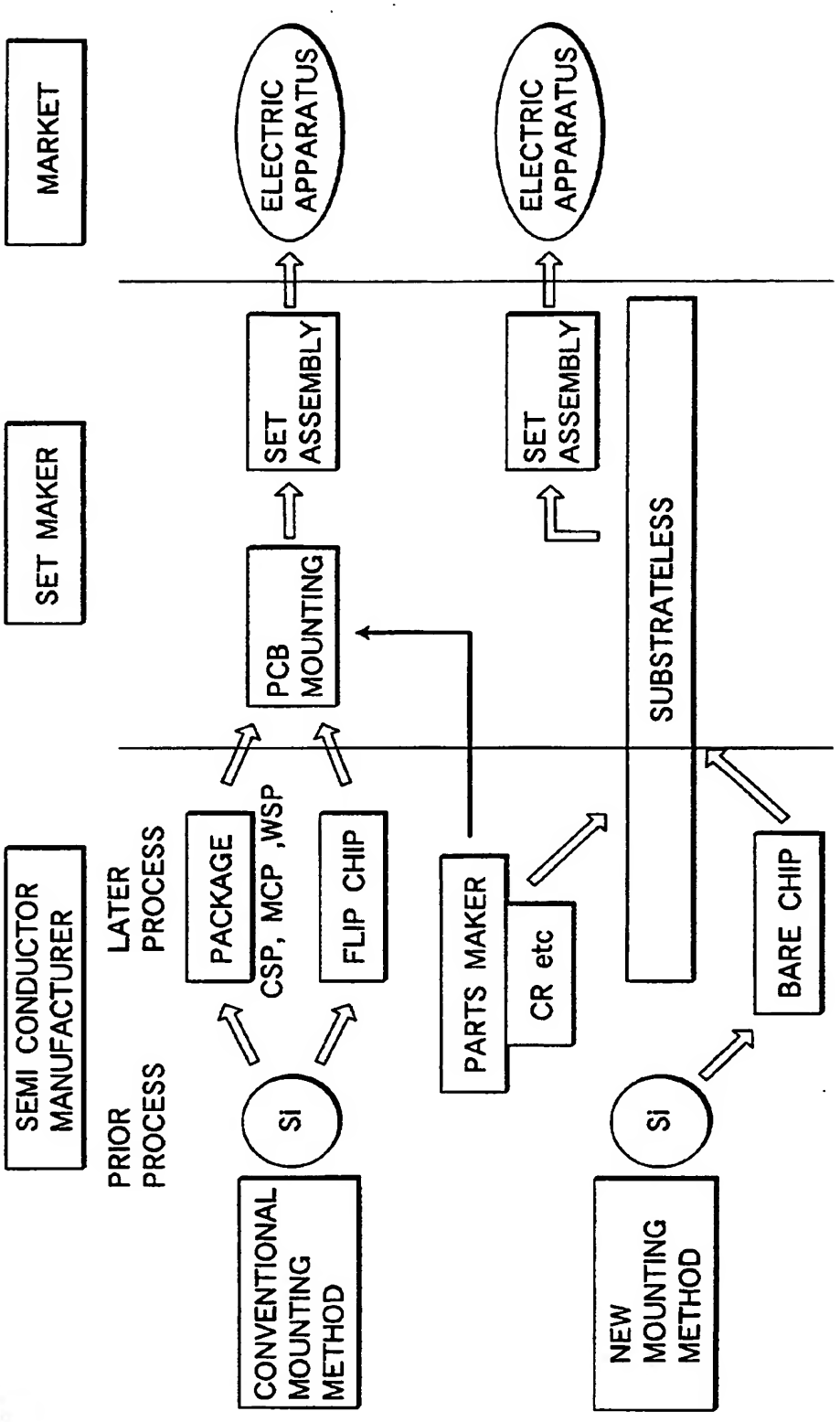


FIG.29


MARKET
SET MAKER
SEMI CONDUCTOR MANUFACTURER
PRIOR PROCESS
LATER PROCESS
CSP, MCP ,WSP
PACKAGE
FLIP CHIP
PCB MOUNTING
SET ASSEMBLY
ELECTRIC APPARATUS
Si
CONVENTIONAL MOUNTING METHOD
PARTS MAKER
CR etc
SUBSTRATELESS
SET ASSEMBLY
ELECTRIC APPARATUS
Si
BARE CHIP
NEW MOUNTING METHOD